

REMARKS

Applicants filed on 06 December 2004 a Response to Final Office Action. In response thereto, an Advisory Action was mailed on 10 January 2005 which denied entry of the amendments proposed in the Response to Final Office Action. Applicants hereby respectfully request entry of the amendments and
5 consideration of the remarks made in the previously-filed Response to Final Office Action, a copy of which is enclosed herewith for the convenience of the Examiner, and Continued Examination.

The Examiner is invited to telephone the undersigned in regard to this Amendment and the above-identified application.

Respectfully submitted,

17-JAN-2005
Date


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CERTIFICATE OF MAILING BY FIRST CLASS MAIL (37 CFR 1.8)

Applicant(s): Jifa Hao, et al.

Docket No.

900065.99R272/17732.6323.00

Application No.

09/654,845

Filing Date

September 1, 2000

Examiner

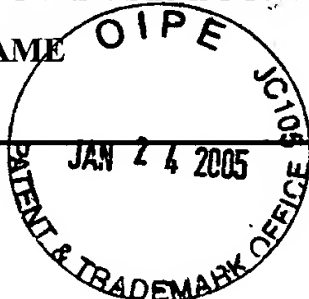
Ori Nadav

Customer No.

34799

Group Art Unit

2811

Invention: **POWER SEMICONDUCTOR DEVICE WITH HIGH AVALANCHE CAPABILITY AND PROCESS FOR FORMING SAME**I hereby certify that this Copy of Previously Filed Response to Final (total 12 pages)*(Identify type of correspondence)*

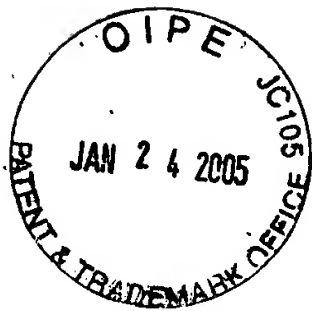
is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope

addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on

January 18, 2005*(Date)*Penny P. Clements*(Typed or Printed Name of Person Mailing Correspondence)*

A handwritten signature in cursive script that reads "Penny P. Clements".

*(Signature of Person Mailing Correspondence)***Note: Each paper must have its own certificate of mailing.**



PATENT
90065.99R272 (17732.6323)
Reply to Final Office Action of 06 Oct. 2004

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

REPLY UNDER 37 CFR 1.116 - EXPEDITED PROCEDURE - EXAMINING GROUP 2811

Applicant: Jifa Hao, et al.)
Serial No.: 09/654,845)
Filed: September 01, 2000)
Title: POWER SEMICONDUCTOR)
DEVICE WITH HIGH)
AVALANCHE CAPABILITY AND)
PROCESS FOR FORMING)
SAME)

COPY

Examiner: Ori Nadav

Art Unit: 2811

RESPONSE UNDER 37 CFR 1.116

MS: AF

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

COPY

Dear Sir:

In response to the Final Office Action mailed 06 October 2004, Applicants hereby submit the following Amendment and Remarks.

IN THE SPECIFICATION

Please amend the title as follows:

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POWER SEMICONDUCTOR DEVICE WITH ~~HIGH AVALANCHE~~ IMPROVED
UNCLAMPED INDUCTIVE SWITCHING CAPABILITY AND PROCESS FOR
FORMING SAME

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IN THE CLAIMS

1. (*Currently Amended*) A power semiconductor device having high avalanche capability, said device comprising:

a semiconductor substrate with two sides surfaces, and an N⁺ doped layer extending into the substrate from one surface ~~of the device into the~~
5 ~~substrate~~ thereof, an N⁻ doped layer over the N⁺ doped layer, a P⁻ doped well formed in the N⁻ doped layer and extending from the other surface of the ~~device~~
substrate into the N⁻ doped layer, a P⁺ doped region formed in the P⁻ doped well and also extending from the other surface of the ~~device~~ substrate into the
P-doped well, the P⁻ doped well defining an upwardly curving junction between
10 the P⁻ doped well and the N⁻ doped layer, said upwardly curving junction extending from ~~the lower end~~ of the P⁻ doped well to the other surface of the
~~device~~ substrate, and an N⁺ doped region formed in the other surface of the
~~device~~ substrate and in the N⁻ doped layer, said N⁺ region laterally spaced from
the P⁺ doped region and the P-doped well, said P⁻ doped well and P⁺ doped
15 region having a combined thickness of about 5 μ m to about 12 μ m; and
recombination centers comprising noble metal impurities disposed
substantially in said N⁻ doped layer and P⁻ doped well.

2. (*Currently Amended*) The device of claim 1 wherein said P - doped well has a thickness of about 4 ~~[[pm]]~~ μm to about 10 μm .

3. (*Currently Amended*) The device of claim 1 wherein said P+ doped region has a thickness of about 0.1 ~~[[gm]]~~ μm to about 2 μm .

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4. (*Previously Presented*) The device of claim 1 wherein said P - doped well has a dopant level of at least 10^{16} atoms/cm³.

5. (*Previously Presented*) The device of claim 4 wherein said P - doped well has a dopant level of about 2.5×10^{17} atoms/cm³.

6. (*Previously Presented*) The device of claim 1 wherein said P+ doped region has a dopant level of at least 10^{18} atoms/cm³.

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7. (*Previously Presented*) The device of claim 6 wherein said P+ doped region has a dopant level of about 6×10^{19} atoms/cm³.

8. (*Currently Amended*) The device of claim 1 wherein said N - doped layer has a dopant level of about 10^{14} atoms/cm³ to about 10^{15} ~~atoms/cm³~~ atoms/cm³.

9. *(Cancelled)*.

10. *(Original)* The device of claim 1 wherein said noble metal impurities are selected from the group consisting of gold, platinum, and palladium.

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11. *(Original)* The device of claim 10 wherein said noble metal impurities comprise platinum.

12. *(Previously Presented)* The device of claim 11 wherein said recombination centers are formed by platinum diffusion through said N + doped substrate into said N - doped and P - doped well.

13. *(Original)* The device of claim 11 containing platinum impurities at a concentration of about 1×10^{15} to about 1×10^{16} atoms/cm³.

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14. *(Original)* The device of claim 13 wherein said concentration of platinum impurities is about 2×10^{15} atoms/cm³.

15. *(Original)* The device of claim 1 further comprising an N + doped region disposed in said N - doped layer.

16. *(Cancelled)*.

17. (*Previously Presented*) The device of claim 16 comprising a diode,
MOSFET or an IGBT power device.

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REMARKS

Claims 1-8, 10-15 and 17-34 are pending in the present application, with claims 9 and 15 having been previously cancelled. Claims 1-8, 10-15 and 17 are rejected and claims 18-34 have been withdrawn from further consideration.

Claims 1-3 and 8 are amended hereby.

5 Claims 1, 2, 3 and 8 are amended hereby for the sake of clarity and format only. Applicants submit that this amendment does not introduce new or remove any limitations, and therefore a new search is not required. Applicants further submit that the proposed amendment places the claims in better condition for Appeal, should that option become necessary. Accordingly, Applicants
10 respectfully request entry of the amendment.

Responsive to the rejection of claims 1-8, 10-15 and 17 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,545,908 (Tokura, et al.) in view of U.S. Patent Nos. 5,063,428 and 5,773,858 (Schlangenotto, et al.), Applicants respectfully traverse.

15 In order to establish a *prima facie* case of obviousness the prior art references must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)(*Emphasis Added*). Claim 1 recites in part,

20 "a P- doped well formed in the N- doped layer and extending . . . into the N- doped layer, a P+ doped region formed in the P- doped well and extending . . . into the P-doped well . . . an N+ doped

region formed . . . in the N- doped layer, said N+ region laterally spaced from the P+ doped region and the P-doped well".

(*Emphasis Added*). Applicants submit that the cited references, alone or in
5 combination, fail to teach or suggest such limitations, and that therefore a *prima facie* case of obviousness has not been established in regard to claim 1.

Tokura, et al., discloses a power MOSFET (Fig. 1) including P-type base
layers 8 having a depth of an of 2.5 μm and N+ type source layers 7 having a
junction depth of an extent of 0.7 μm . (*column 10, lines 45-49*). P+ type base
10 contact layers 10 have a diffusion depth of 0.5 μm are formed on a surface of a
central portion of the p-type base layer 8. (*column 10, lines 57-60*).

The N+ sources 7 and P+ base contact layers 10 of the Tokura, et al.,
device are formed within P-type base layers 8. Tokura, et al., itself teaches that
the N+ sources are formed within the P-type base layers 8. The N+ regions are
15 not laterally spaced or separated from the P-type base layers 8. There is no N+
region laterally spaced or separated from the P-type base layers 8. Thus,
Tokura, et al., fails to disclose or suggest an N+ doped region formed in the N-
doped layer and being laterally spaced from the P+ doped region and the P-
doped well, as recited in part by claim 1.

20 The Schlangenotto, et al., references were not relied upon by the
Examiner to, and Applicants submit they do not, teach, disclose or suggest an N+

doped region formed in the N- doped layer and being laterally spaced from the P+ doped region and the P-doped well, as recited in part by claim 1.

Since the cited references fail to disclose or suggest, alone or in combination, all the limitations of claim 1, Applicants submit that a *prima facie* case of obviousness has not been established in regard thereto. Accordingly, Applicants respectfully request withdrawal of the rejection and submit that claim is now in condition for allowance, which is hereby respectfully requested.

In rejecting claim 1 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,545,908 (Tokura, et al.) in view of U.S. Patent Nos. 5,063,428 and 5,773,858 (Schlangeneotto, et al.), the Examiner in regard to the Tokura, et al., device parenthetically asserts the following: "the N+ doped region (7) is formed in a P doped well (8), and the P doped well (8) is formed in the N-doped layer (2). Therefore, the N+ doped region is formed in the N- doped layer." (bottom of Page 2 through the top of Page 3 of the Office Action mailed 06 October 2004). Applicants respectfully disagree.

The Examiner appears to be concluding that because the P doped well (8) is formed in the N- doped layer (2), and since the N+ doped region (7) is, in turn, formed in the P doped well (8), that the N+ doped region (7) is therefore formed in the N- doped layer (2). With all due respect to the Examiner, such an oversimplification ignores semiconductor physics, operation, and fabrication methods. If such a generalization were adhered to, e.g., all features of a

semiconductor are formed on the substrate, countless semiconductor patents would be rendered invalid. The presence of the P doped well can not be ignored.

The P doped well (8) of Tokura, et al., is formed in the N- doped layer (2), and the N+ doped region (7) is, in turn, formed in the P doped well (8). The N+ doped region (7) is not formed in the N- doped layer (2). Rather, the N+ doped region (7) is formed within the P doped well (8). It is the P doped well (8) that is formed in the N- doped layer (2), not the N+ doped region (7). The N+ doped region (7) is formed within P doped well (8), not within the N- doped layer (2).

Further, to conclude that the N+ doped region is formed in the N- doped layer 2 ignores the teaching of Tokura, et al. Tokura, et al., implants boron ions to form p-well 61 (Fig. 7) and deep p- well 60 which are made into a unitary body to produce composite p- well 62. (*column 12, lines 46-53*). Next, a second ion injection and diffusion are formed to create n+ type source layer 7. (*column 13, lines 1-15*). Thus, the very teaching of Tokura, et al., requires that the P doped well (8) be formed in the N- doped layer (2), and that the N+ doped region (7) be, in turn, formed in the P doped well (8).

In contrast, the explicit language of claim 1 requires that the N+ doped region of Applicants' invention be formed in the N- doped layer. The N+ doped region of the present invention is not formed in a P doped well which is, in turn, formed in an N- doped layer. Thus, Tokura, et al., fails to disclose or suggest an

N+ doped region formed in the N- doped layer and being laterally spaced from the P+ doped region and the P-doped well, as recited in part by claim 1.

The Schlangeneotto, et al., references were not relied upon by the Examiner to, and Applicants submit they do not, teach, disclose or suggest an N+
5 doped region formed in the N- doped layer and being laterally spaced from the P+ doped region and the P-doped well, as recited in part by claim 1.

For the foregoing reasons, Applicants submit that claim 1 and claims 2-8, 10-15 and 17 depending therefrom are now in condition for allowance, which is hereby respectfully requested.

10 For all the foregoing reasons, Applicants submit that the pending claims are definite and do particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Moreover, Applicants submit that the pending claims are also now in condition for allowance. Accordingly, Applicants respectfully request withdrawal of all rejections and allowance of the claims.

15 In the event Applicant has overlooked the need for an extension of time, additional extension of time, payment of a fee, or additional payment of a fee, Applicant hereby conditionally petitions therefor.

The Examiner is invited to telephone the undersigned in regard to this
Amendment and the above identified application.

Respectfully submitted,

6-DEC-2004
Date


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